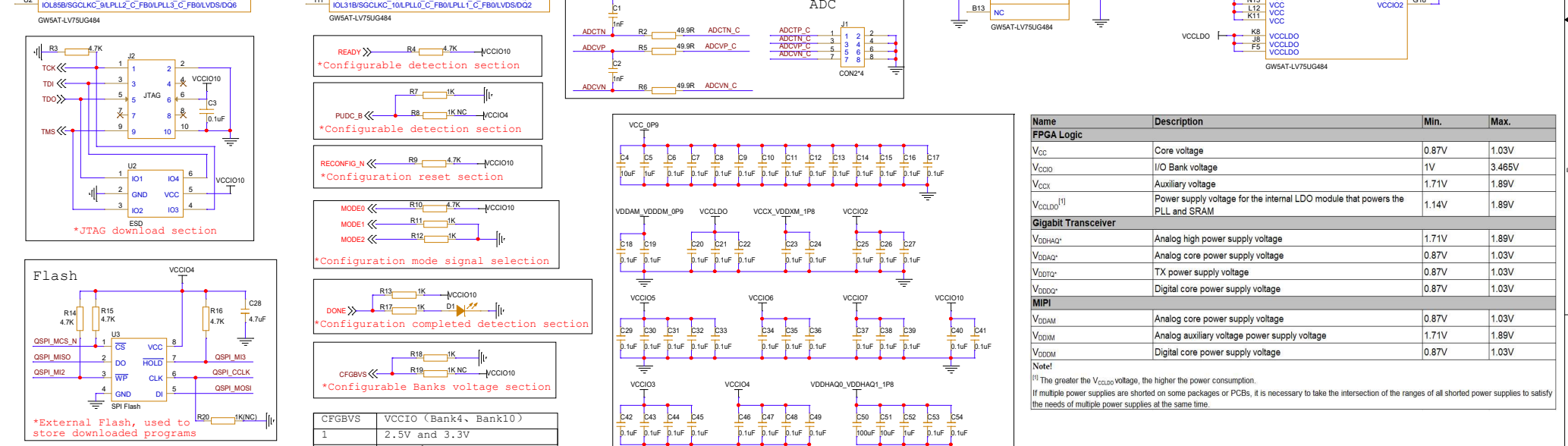
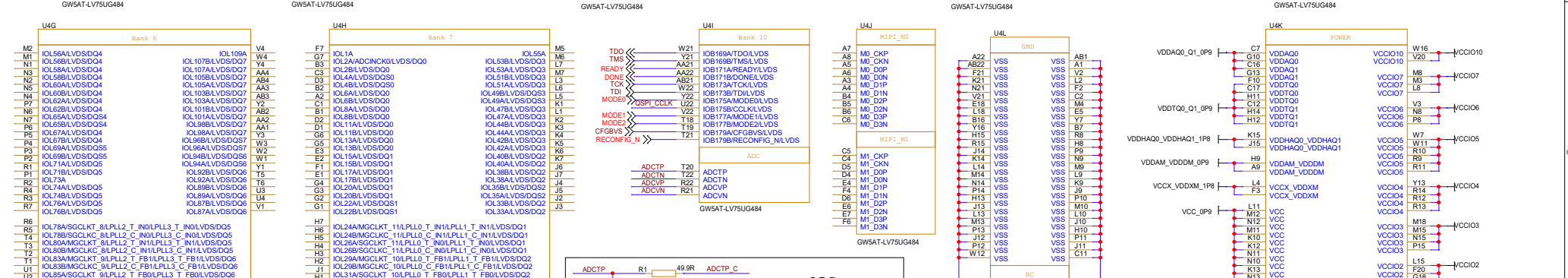
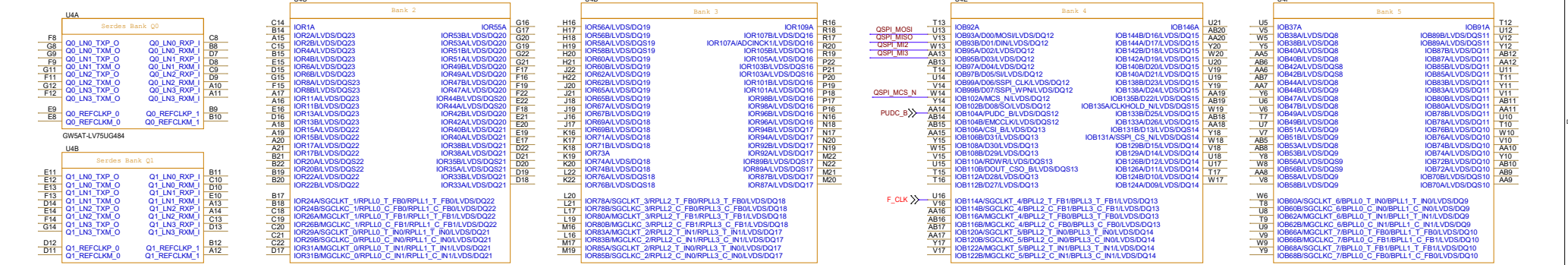


GW5AT-LV75UG484



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage	0.87V	1.03V
V _{CCIO}	I/O Bank voltage	1V	3.465V
V _{CCX}	Auxiliary voltage	1.71V	1.89V
V _{CCLD0} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
Gigabit Transceiver			
V _{DDHAQ} *	Analog high power supply voltage	1.71V	1.89V
V _{DDIAQ} *	Analog core power supply voltage	0.87V	1.03V
V _{DDTQ} *	TX power supply voltage	0.87V	1.03V
V _{DDDQ} *	Digital core power supply voltage	0.87V	1.03V
MIPI			
V _{CCDM}	Analog core power supply voltage	0.87V	1.03V
V _{DDIM}	Analog auxiliary voltage power supply voltage	1.71V	1.89V
V _{DDDM}	Digital core power supply voltage	0.87V	1.03V
Note!			
^[1] The greater the V _{CCLD0} voltage, the higher the power consumption.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

Notes:

1. F_CLK signal is an external input clock signal.
2. External Flash memory is used to store downloaded programs.
3. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in the Arara V FPGA Products Programming and Configuration Guide.
4. It is recommended that add an ESD protection chip to the JTAG download circuit.
5. VCC core voltage requires a large current, so it is recommended to supply power separately.
6. The MODE pin is the GowinCONFIG configuration mode selection signal.
7. For details about how to select the Mode signal, see "Section 3.1 Configuration Modes" in the Arara V FPGA Products Programming and Configuration Guide.